UM10058

ISP1504 ULPI transceiver evaluation board, supporting Hi-Speed USB host, peripheral and OTG

Rev. 01 — 1 June 2006 User manual

Document information

Info	Content
Keywords	isp1504, usb, ulpi, universal serial bus, transceiver, utmi+ low-pin interface, host, peripheral, otg, usb 2.0, phy
Abstract	The document describes how the ISP1504 eval board can be configured to interface with link to provide a USB physical layer front-end solution. This document also includes the schematic of the eval board and the components needed to integrate the ISP1504 to the user's system.

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Revision history

Rev	Date	Description
01	20060601	First release.

Contact information

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1. Introduction

The ISP1504 is an 8-bit bidirectional UTMI+ Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to implement as a Hi-Speed USB host, peripheral or OTG device.

The ISP1504 evaluation (eval) board allows designers to evaluate the features of the ISP1504, and conduct system-level validation and testing. The eval board interfaces to the link through a 100-pin Transceiver and Macrocell Tester (T&MT) connector that complies with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2*.

Fig 1 shows the ISP1504 eval board.

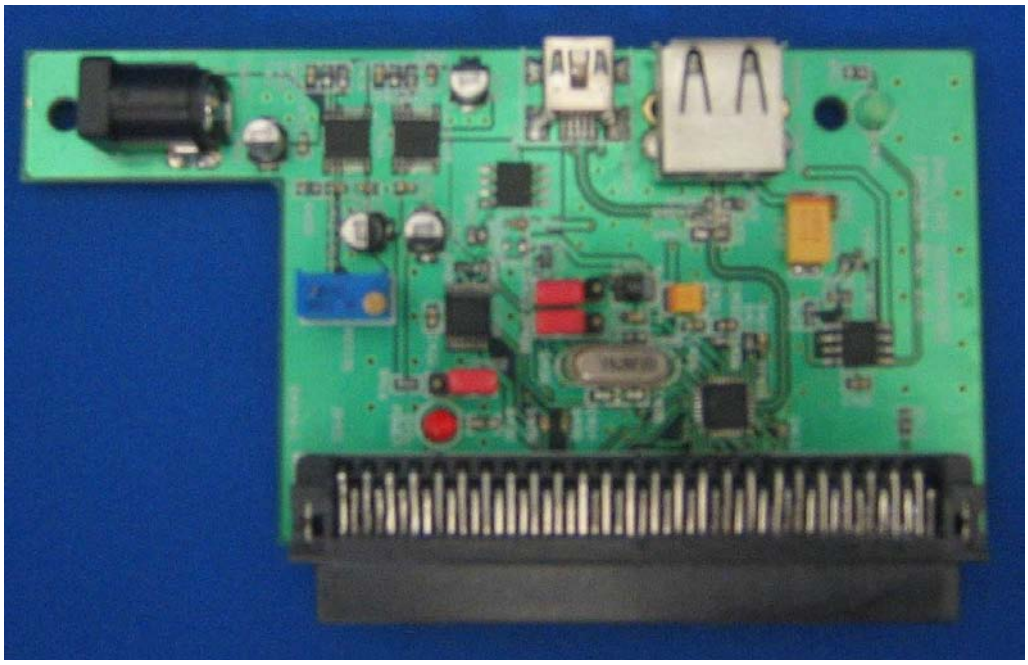


Fig 1. ISP1504 eval board

2. Board features

2.1 Functionality

- The ISP1504 is fully compliant with *Universal Serial Bus Specification Rev. 2.0, UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1* and *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a.*
- The T&MT connector interface is fully compliant with *USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2.*
- The V_{BUS} power can be supplied either by the on-chip charge pump or by the on-board power switch.
- Configurable active-HIGH or active-LOW reset signal from the link.
- Adjustable V_{CC} voltage when powered by the 5 V DC power supply.
- Configurable CHIP_SEL_N signal.

- Flexible clock source for the ISP1504: on-board crystal, 60 MHz input clock or square wave clock driven into the XTAL1 input.

2.2 Connectors

- USB connectors: standard-A (mounted by default), standard-B and mini-AB (mounted by default)
- T&MT connector to interface to the link
- Input power connector

2.3 Power supplies

- Supplied by the 5 V DC power supply through the input power connector, or
- Supplied by the link through the T&MT connector

3. Board usage

3.1 Overview

The ISP1504 eval board is designed to connect to a link board through the T&MT connector for system validation as shown in Fig 2.

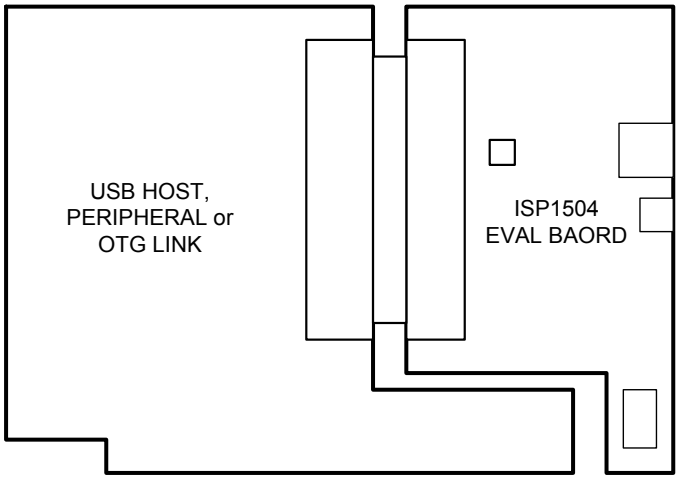
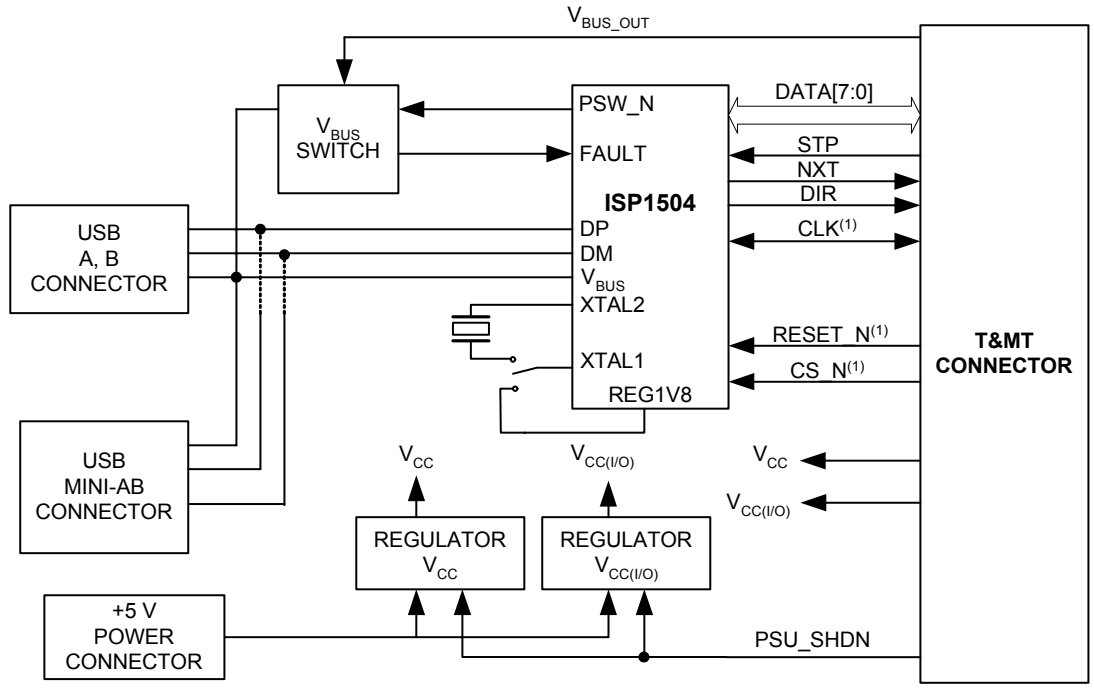


Fig 2. ISP1504 eval board connected to the link board

3.2 Block diagram

Fig 3 shows the high-level block diagram of the ISP1504 eval board.



(1) These pins are multiplexed with other functions. Only one function, however, can be used at one time.

Fig 3. ISP1504 eval board block diagram

3.3 Power supply

The ISP1504 eval board can be powered either from the input power connector (SW400) or from the T&MT connector (JP401). When power is supplied from the link through the T&MT connector, pin 100 of the connector must be connected to ground on the link side. This will shut down the V_{CC} and $V_{CC(I/O)}$ regulator outputs to the ISP1504. When power is supplied from the input power connector, pin 100 of the T&MT connector must be left open on the link side.

There are two regulators on the eval board supplying V_{CC} and $V_{CC(I/O)}$. Regulator IC404 supplying V_{CC} has an adjustable output voltage, which must be set to a voltage between 3.0 V and 3.6 V by tuning POT101. Regulator IC405 supplying $V_{CC(I/O)}$ has a fixed output voltage of 3.3 V. Solder bridges S412 and S406 must always be closed. LED D401 indicates the existence of V_{CC}.

3.4 V_{BUS} is supplied by the internal charge pump

A host or an OTG A-device needs to supply V_{BUS}. The ISP1504 has a built-in charge pump, which can supply up to 50 mA current to V_{BUS}. If the downstream device draws less than 50 mA current from the ISP1504, the built-in charge pump feature can be used to save the cost on external components. No hardware changes need to be made to the eval board to evaluate the internal charge pump of the ISP1504. Table 1 lists the register bits that must be configured to utilize the internal charge pump.

Table 1. Register bits related to the internal charge pump

Register	Remark
DRV_VBUS	Set to turn on the internal charge pump. Cleared to turn off the internal charge pump
DRV_VBUS_EXT	Must be cleared (default)

3.5 V_{BUS} is supplied by the external power switch

The internal charge pump of the ISP1504 can supply a maximum of 50 mA current. If more than 50 mA current will be drawn from the device, an external power switch or a charge pump is required. *Universal Serial Bus Specification Rev. 2.0* allows continuous shorting between V_{BUS} and ground. Therefore, the power switch or the charge pump is required to detect overcurrent condition and thermally shut down. So, an external active-LOW enabled power switch or a charge pump with digital fault output, for example, MIC2026-2, is required. On the eval board, an external power switch (IC407) with digital fault output is implemented. To use the external V_{BUS} power switch, the eval board must be configured as follows:

1. Short solder bridge S404 and open solder bridge S403 to route 5 V to the input of the power switch (pin 7 of IC407).
2. Short solder bridge S410 and open solder bridge S411 to connect fault output of the power switch to the ISP1504 FAULT input.

The link must supply 5 V to the power switch through pin 28 of the T&MT connector.

Table 2 lists the register bits that must be configured to utilize the external power switch. When the DRV_VBUS_EXT register bit is set, the ISP1504 will output LOW on PSW_N (pin 12 of IC400) to turn on the power switch. Once the V_{BUS} power switch is turned on, green LED D400 will light up.

Table 2. Register bits related to the external charge pump

Register	Remark
DRV_VBUS_EXT	Set to turn on the external charge pump Cleared to turn off the external charge pump
DRV_VBUS	Cleared (power on default value)
USE_EXT_VBUS_IND	Set to detect fault condition output from the external power switch
IND_COMPL	Set if the fault output from the power switch is active HIGH. Cleared if it is active LOW

3.6 USB connectors

There are two USB connectors mounted on the eval board by default, standard-A USB connector and mini-AB USB connector. For a peripheral application, the standard-B connector must replace the standard-A USB connector.

The DP and DM lines are switched between the two USB connectors using a 0 Ω link resistor to achieve better signal quality. If the eval board is used for a host or peripheral application, DP and DM of the ISP1504 must be routed to the DP and DM pins of the standard-A or standard-B USB connector, respectively. In this case, R401 and R402 must be mounted, and R403 and R404 must be removed (default). If the eval board is used for an OTG application, DP and DM of the ISP1504 must be routed to the DP and

DM pins of the mini AB connector, respectively. In this case, R403 and R404 must be mounted, and R401 and R402 must be removed.

For a peripheral application, the capacitance on V_{BUS} must be limited to be less than 10 µF so that there will not be a large in-rush current when connected. Therefore, solder bridge S402 must be removed. For a host application, however, solder bridge S402 must be closed so that the 100 µF filter capacitor will prevent the voltage on V_{BUS} from dropping below 4.5 V, when a downstream device is connected.

3.7 CHIP_SEL_N

The CHIP_SEL_N pin of the ISP1504 allows the ULPI interface to be shared with other ICs. Driving the CHIP_SEL_N pin to LOW will 3-state the DATA, NXT and DIR pins. Therefore, other ICs can use these pins.

On the eval board, CHIP_SEL_N is permanently shorted to ground by installing a jumper on pins 2 and 3 of JP402 (default). It can, however, be controlled from the link by removing the jumper and closing solder bridge S405. Therefore, the link can select or de-select the ISP1504 by driving pin 18 of the T&MT connector to either LOW or HIGH.

3.8 RESET_N

The reset signal of the ISP1504 is an active-LOW asynchronous input that resets all internal circuitry. On the eval board, an invert is inserted between RESET_N of the ISP1504 and pin 17 of the T&MT connector, if S401 is closed and S400 is opened. This provides the flexibility in designing the link. If reset from the link is an active-HIGH signal, it can be inverted on the eval board by closing S401 and opening S400. Otherwise, S401 must be opened and S400 must be closed.

If the link chooses not to reset the ISP1504, pin 17 of the T&MT connector can be shorted to ground on the link side, provided S400 is opened and S401 is closed. Alternatively, pin 17 of the T&MT connector can be pulled HIGH with S400 closed and S401 opened.

3.9 Clock supply

There are three ways to provide a clock to the ISP1504:

- Attach a crystal between XTAL1 and XTAL2 (pins 15 and 16). In this case, a jumper must be installed between pin 1 and pin 2 of JP400. The value of the crystal depends on the silicon version.
- Drive an external clock into the XTAL1 pin. In this case, the jumper on pin 1 and pin 2 of JP400 must be removed and an external clock source must be applied on pin 2 of JP400. The value of the external clock depends on the silicon version.
- Drive a 60 MHz clock into CLOCK (pin 27 of the ISP1504). In this case, the jumper on pin 1 and pin 2 of JP400 must be removed and 1.8 V must be applied to pin 2 of JP400 (the REG1V8 output can be connected to this pin). Therefore, the CLOCK pin of the ISP1504 functions as an input on power-up and the link can drive 60 MHz clock into this pin.

3.10 Pull-up resistor on DM

For a low-speed peripheral application, DM must be pulled up. This can be achieved by turning on the external 1.5 kΩ pull-up resistor by using controller LS_Enable (pin 20 of JP401). Inverter IC406A is required if the low-speed enable is active HIGH because the gate of the PMOS switch must be LOW to route 3.3 V to the pull-up resistor. S407 and

S409 provide the flexibility to bypass or use the inverter. Header JP403 allows to manually control the DM switching, without the low-speed enable.

3.11 Configuration summary

A summary of the eval board configurations for various applications is given in Table 3.

Table 3. Summary of the transceiver configuration for various applications

Configurable setting		Host application	Peripheral application	OTG application
DP and DM routing	R401 and R402	Mounted	Mounted	Not mounted
	R403 and R404	Not mounted	Not mounted	Mounted
V_{BUS} capacitance	S402	Closed	Open	Open
V_{BUS} power switch	S404	Closed	Open	Open
	S410	Closed	Open	Open
Reset control	S400	Closed	Closed	Closed
	S401	Open	Open	Open
$V_{CC(I/O)}$ power	S412	Closed	Closed	Closed
Crystal selection	JP400	Installed on pins 1 and 2	Installed on pins 1 and 2	Installed on pins 1 and 2
Chip selection	JP402	Installed on pins 2 and 3	Installed on pins 2 and 3	Installed on pins 2 and 3
	S405	Open	Open	Open

Remark: Solder bridges S403 and S411 are for earlier versions of the ISP1504 and should never be used (leave open). The settings in Table 3 assume high-speed operation with an on-board crystal as the clock source. The settings also assume that the ISP1504 is permanently selected.

4. Quick troubleshooting guide

Following is a step-by-step guide to troubleshoot the ISP1504 eval board, if you encounter any problem.

1. Check the printing on the IC package to ensure that you have the latest revision. The last letter on the third line indicates the revision of the chip.
2. Power the eval board through the SW400 connector with a 5 V power supply.
3. Measure the voltage at V_{CC}. It must be between 3.0 V and 3.6 V. Measure the voltage at $V_{CC(I/O)}$. It must be around 3.3 V. If both regulators give no output, check whether PSU_SHDN is pulled up to 5 V. If only one regulator gives abnormal output, it is likely that the regulator is faulty.
4. Measure the voltage at the RREF pin of the ISP1504. The voltage must be around 1.20 V to 1.27 V. If the voltage at the pin is abnormal, it is likely that the chip is not properly soldered on the PCB or the IC is damaged.
5. Measure the output voltage at REG1V8 and REG3V3. These voltages must be 1.8 V and 3.3 V, respectively. If the voltage at these pins is abnormal, it is likely that the IC is damaged.
6. Ensure that configuration settings are as given in Table 3.

7. Probe the CLOCK pin of the ISP1504 with an oscilloscope. A 60 MHz clock must be observed. If there is no output on the CLOCK, check if the chip is selected, that is, a jumper must be installed on pins 2 and 3 of JP402.
8. If the link cannot perform any TXCMD, check whether the RESET_N pin is HIGH during operation.
9. If the high-speed eye pattern fails, try a few samples to confirm that it is not a soldering issue.
10. If the preceding steps do not help resolve the problem, send e-mail to customer support at wired.support@philips.com, quoting the chip version, chip revision and board information.

5. PCB guideline

The ISP1504 eval board has four layers. The top and bottom layers consist of signal, power tracks and ground fill, while the second and third layers are power and ground planes.

It is recommended that you follow these guidelines when designing a PCB:

- To get stable band gap reference V_{REF}, place the R_{RREF} resistor R400 close to pin 3 of the ISP1504. The 12 kΩ resistor connected to R_{RREF} must have a tight tolerance 1 % or better.
- The charge pump capacitor (C400) must be placed close to pin 9 (C_B) and pin 10 (C_A) to minimize the capacitance from the trace line that will affect the amount of charge pump current drawn.
- Place decoupling capacitors close to the supply pins of the ISP1504. Each $V_{CC(I/O)}$ pin must be decoupled using one decoupling capacitor. If there is a high-radiated emission, ferrite beads can be used, and must be placed close to supply pins $V_{CC(I/O)}$ and V_{CC}. Ferrite beads used in the application can be between 50 Ω and 120 Ω at 100 MHz, with a current rating of approximately 200 mA.
- Place decoupling and filtering capacitors close to the output pins of the 1.8 V and 3.3 V regulators.
- Place the crystal oscillator and two load capacitors close to XTAL1 and XTAL2 of the IC to avoid unstable oscillation because of resonance from parasitic inductance and capacitance.
- To achieve differential impedance of 90 Ω on the DP and DM lines, the trace width and spacing of DP and DM must comply with *Universal Serial Bus Specification Rev. 2.0* requirement of 7.5 mils width and 7.5 mils spacing. Also, the parallelism of the DP and DM lines must be maintained. Avoid stubs on lines.
- Ground vias are recommended for ground plane interconnect and must be kept apart by a maximum distance of 10 mm x 10 mm.
- The exposed die pad at the bottom of the ISP1504 is a ground and therefore, must be grounded on the PCB board for the transceiver to function properly.
- Route the clock out away from the data line to avoid crosstalk. If the clock signal is distorted by reflection, a series termination resistor can be considered. The termination resistor must be placed closed to the clock source.

6. Components required when integrating

Table 4 provides components that are required when integrating the ISP1504 into the system. For more information, refer to the ISP1504 data sheet.

Table 4. Components required when integrating the ISP1504

Designator	Component description	Location	Value	Remark
R400	Resistor for band gap reference	On RREF (pin 3)	12 kΩ ± 1 %	-
C400	Charge pump capacitor	Between C_B and C_A (pins 9 and 10)	270 nF	To supply up to 50 mA current
C401	Filter capacitor	On V_{BUS} (pin 13)	See Table 5	-
C402	Decoupling capacitor	On REG3V3 (pin 14)	100 nF	-
C403	Filtering capacitor	On REG3V3 (pin 14)	4.7 µF	-
Q400	Crystal oscillator	Between XTAL1 and XTAL2 (pins 15 and 16)	ISP1504A: 19.2 MHz ± 50 ppm ISP1504C: 26 MHz ± 50 ppm	Recommended crystal spec: Crystal drive level: 500 µW max; ESR ≤ 100 Ω max; shunt package capacitance = 7 pF max.
C404, C405	Load capacitor	Between XTAL1 and ground and XTAL2 and ground (pins 15 and 16)	18 pF	Not required if using clock from another source
C406	Decoupling capacitor	On REG1V8 (pin 18)	100 nF	-
C407	Filter capacitor	On REG1V8 (pin 18)	4.7 µF	-
C408	Decoupling capacitor for $V_{CC(I/O)}$	On each $V_{CC(I/O)}$ pin (pins 2, 22 and 30)	100 nF	-
C424	Decoupling capacitor for V_{CC}	On V_{CC} (pin 11)	100 nF	-
IC407	V_{BUS} power switch	Between FAULT AND PSW_N	V_{BUS} power switch or charge pump with digital fault output	Required only if the host is driving more than 50 mA on V_{BUS}
R412	Pull-up resistor	On PSW_N (pin 12)	10 kΩ	Required if V_{BUS} power switch is needed

Table 5. Recommended V_{BUS} capacitor

These values are according to the Universal Serial Bus Specification Rev. 2.0 and On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a requirements.

CV_{BUS}	Min	Max	Unit
Host	-	120	µF
OTG	1	6.5	µF
Peripheral	1	10	µF

7. Schematics

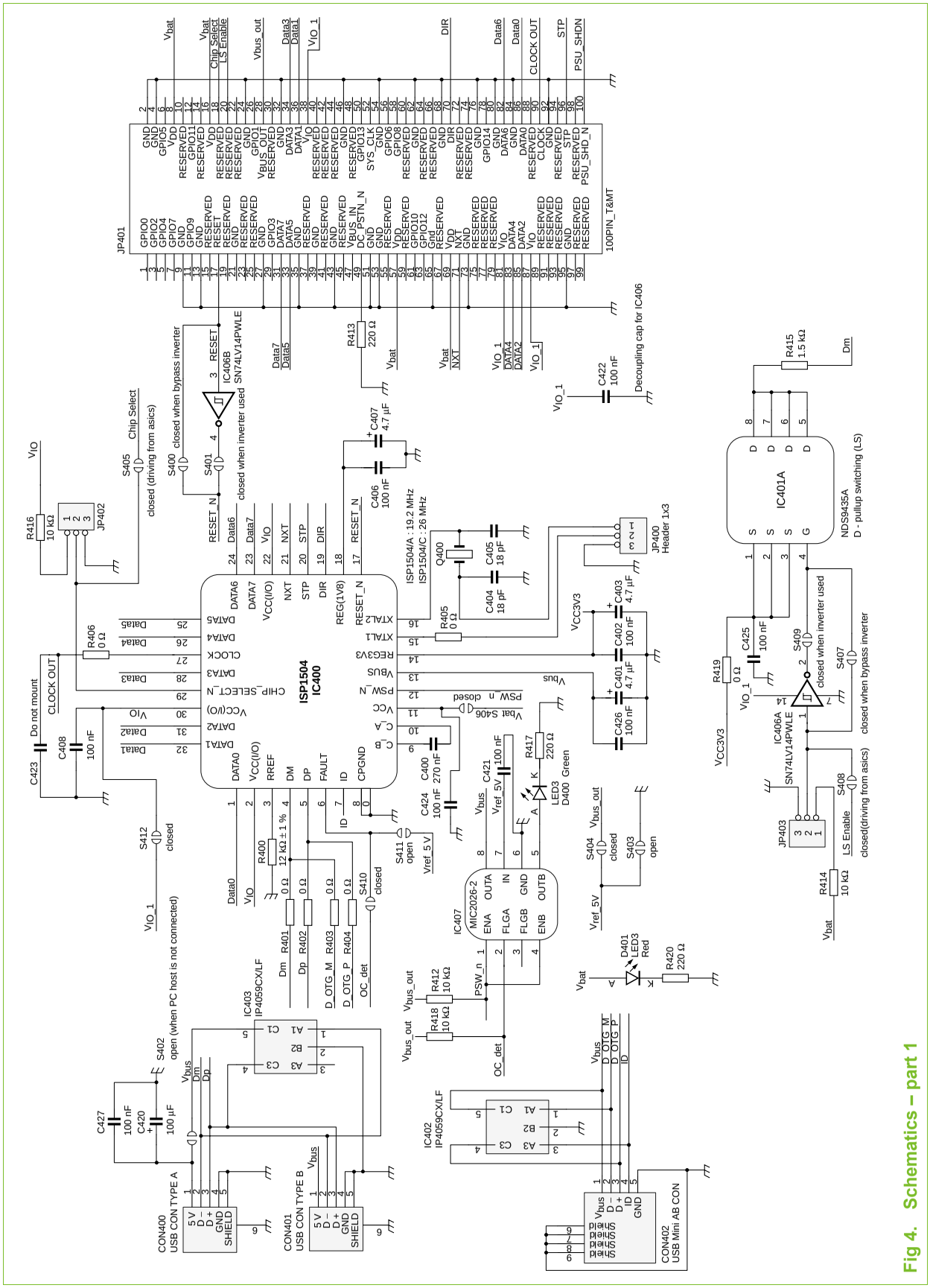


Fig 4. Schematics – part 1

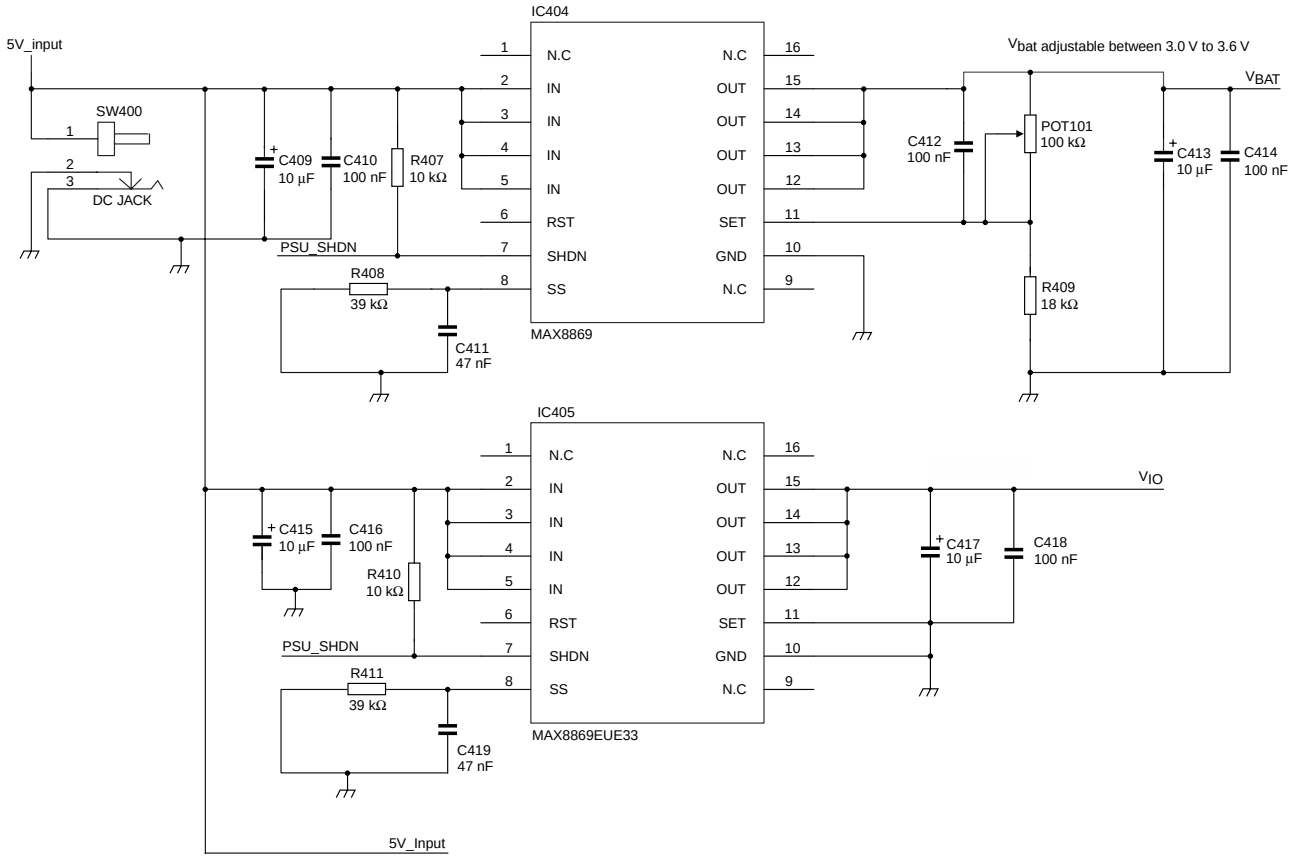


Fig 5. Schematics – part 2

8. Bill of materials

Table 6. Bill of materials

Designator	Footprint	Comment
R401 R402 R403 R404 R405 R406 R419	0603	0 Ω
R407 R410 R412 R414 R416 R418	0603	10 kΩ
C408 C410 C412 C414 C416 C418 C421 C423 C424 C425 C426 C427 C402 C406	0603	100 nF
R400	0603	12 kΩ ± 1%
R409	0603	18 kΩ
R415	0603	1K5
C404 C405	0603	18 pF
R413 R417 R420	0603	220 Ω
C400	0603	270 nF
R408 R411	0603	39 kΩ
C411 C419	0603	47 nF
JP401	2-557101-5	100PIN_T&MT
C401 C403 C407	CASE B	4.7 µF
C420	CASE D	100 µF
Q400	Crystal	19.2 MHz
SW400	DC JACK	DC JACK
C409 C413 C415 C417	ECASE-B	10 µF
IC400	HVQFN32-SMT	ISP1504
IC402 IC403	IP4059CX5	IP4059CX/LF (optional)
S400 S401 S402 S403 S404 S405 S406 S407 S408 S409 S410 S411 S412	SIP2-S	SIP2-S
JP400 JP402 JP403	SIP3	Header 1x3
IC401	SO-8	NDS9435A
IC404	TSSO5X6-G16	MAX8869
IC405	TSSO5X6-G16	MAX8869EUE33
IC406	TSS05x6-G14/X.3	SN74LV14PWLE
IC407	SOP_8	MIC2026
CON400	USB_A	USB CON TYPE A
CON402	USB_AB	USB Mini AB receptacle

Designator	Footprint	Comment
CON401	USB_B	USB CON TYPE B
POT101	VARR	100 kΩ
D400 D401	3MM_LED	LED3

9. Abbreviations

Table 7. Abbreviations

Acronym	Description
OTG	On-The-Go
T&MT	Transceiver and Macrocell Tester
ULPI	UTMI+ Low Pin Interface
UTMI	USB 2.0 Transceiver Macrocell Interface
USB	Universal Serial Bus

10. References

- Universal Serial Bus Specification Rev. 2.0
- On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0a
- ISP1504 ULPI Hi-Speed Universal Serial Bus On-The-Go transceiver data sheet
- UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1
- USB 2.0 Transceiver and Macrocell Tester (T&MT) Interface Specification Ver. 1.2

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